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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,751	04/13/2001	Sergey A. Velichko	303.750US1	4280

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EXAMINER	
MILLER, CRAIG S	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,751	VELICHKO ET AL.	
	Examiner	Art Unit	
	Craig Miller	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed 2/11/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-58 are rejected under 35 U.S.C. § 103(b) as being unpatentable over Ekstedt *et al.* in view of Tong and Yun (6,240,331 B1).

As to claims 1, 2, 6-9, 16, 19-22, 29, 30, 34-37, 44, 45, 49-52, Ekstedt *et al.* discloses a control module (fig. 8 and [16]) to control concurrently operation of the semiconductor test equipment and operation of parametric test instrumentation (functional block [76] of fig. 9). Ekstedt *et al.* specifies neither that the disclosed functions should be embodied within a computer (machine) readable medium nor that the control of the test equipment and the parametric test equipment should be co-controlled concurrently. Yun discloses a semiconductor process control system integrated management system which discloses inter-process data sharing (top of col. 3) and central process control (col. 4 lines 4+ and item [317]) and that this control includes central control host computer [130] directs processing in the semiconductor fabricating equipment (bottom of col. 2). Yun specifies that the process control equipment include semiconductor manufacturing and subsequent manufactured circuit testing (top of col. 3). Because the functions of Ekstedt *et al.* are disclosed as being computer implemented and because it is well known that such computer functions are implemented via computer readable code, see Arackaparambil *et al.* (US Pre-pub. 2002/0156548 A1, priority date: 7/29/1999) abstract and paragraph 15, "*Accordingly, a need exists for methods and techniques which provide improved computer implemented integration of semiconductor manufacturing techniques in order to optimize process control, quality, yield and cost reduction. Also, there is a need for centralized wafer fab management and control through a computer integrated manufacturing system which facilitates processing or equipment changes without extensive software programming.*" and because it is well known that such code is commonly embodied upon computer readable media, see Rinnen *et al.* (5,943,230), see bottom of col. 4, "*Processor 22 executes system control software, which is a computer program stored in a computer-readable medium such as memory 23.*", it would have been obvious to one of ordinary skill in the art at the time the invention was made that the computer functions of Ekstedt *et al.* should be embodied upon

computer readable media so as to receive the expected benefits derived there from such as enhanced system flexibility, the computer control of the circuit testing and parametric testing being co-controlled (fig. 9). As to concurrently controlling the test equipment and the parametric test equipment, Tong discloses the state of the art at the time the invention was made in computer aided scheduling systems. Tong discloses in the abstract that one should identify all job scheduling conflicts (fig. 1, identifying job scheduling conflicts in item [104] and adjusting the job priorities to systematically eliminate such conflicts in items [106], [108], [110], [112] and [114]), compute priority indexes for each conflict [106], and for each step, calculate flexibility index [108] and hold fixed inflexible steps [110]. Because the device of Ekstedt *et al.* as modified above discloses a production system, because Tong discloses that conflicts should be prioritized and conflicts should be eliminated, because Ekstedt *et al.* discloses that data processing may be performed offline (col. 11 line 42+) , because Yun teaches that semiconductor manufacturing and subsequent circuit testing equipment should be co-controlled and because it is well known within the art of computer process monitoring that programs may be pre-loaded or post-processed, *see* Eksted *et al.* (5,206,582) col. 11, *"If specified as part of the test procedure, the general test program can also format and transmit measurement results to a database for off-line data analysis."*, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the process of Ekstedt *et al.* as modified above prioritized co-control, the offline processing of Ekstedt *et al.* being clearly not found in conflict with the other wafer manufacturing jobs if one of ordinary skill in the art at the time the invention was made if one utilized the known job prioritization scheme of Tong. Furthermore, the use of disclosed and/or known post or pre-processing which are known not to conflict with wafer manufacturing are therefore reasonably considered concurrent processes under simultaneous control absent a showing of unexpected results or synergistic effect from any particular claimed combination.

As to claims 4, 5, 17, 18, 32, 33, 47 and 48 Ekstedt *et al.* discloses a prober [13] and parametric measurement instruments [10].

More particularly with respect to claims 44, 45 and 47-52, said claims are directed towards computer (machine) readable media. Because the functions of Ekstedt *et al.* are disclosed as

being computer implemented, particularly with a general test computer program (fig. 2), it is deemed inherent that such computer programs shall reside upon computer readable media such as fixed disk hardrives.

As to claims 3, 31 and 46, said claims are directed towards implementing the control functions within electronic hardware. The use of electronic hardware is well known within the IC test arts for testing circuits, see Hollander et al. (6,675,138 B1, priority to 6/8/1999). *"The method of the present invention could also be described as a plurality of instructions being performed by a data processor, such that the method of the present invention could be implemented as hardware, software, firmware or a combination thereof..."*. Programmed hardware implementing test functions are well known functional equivalents to software implemented test functions and are often used when changes in test programs are not of main concern. Therefore, because Ekstedt *et al.* does not preclude the performance of the test functions within pre-programmed electronic hardware and because Applicants fails to claim any particular unexpected result or synergistic effect from such use, it would have been obvious to one of ordinary skill in the art at the time the invention was made that pre-programmed electronic hardware could be substituted for the software programmable functions of Ekstedt *et al.*, each performing similar functions in similar ways, so as to receive the expected benefits derived there from such as enhanced system reliability.

As to claims 10, 11, 13-15, 23, 24, 26-28, 38, 39, 41-43, 53, 54 and 56-58, said claims are directed towards the control module controlling the test state via a state oscillator module controlling other modules. Ekstedt *et al.* as modified above discloses the instant invention with the exception that Ekstedt *et al.* as modified above does not specify that the control module synchronously sets the test state through a state oscillator module. Ekstedt *et al.* discloses in col. 4 that any appropriate test may be performed by the invention. The Examiner takes notice that parametric testing of ICs is commonly performed with clock synchronization of test modules, see Lesmeister (5,931,952) *"Thereafter a clock signal transmitted to all of the nodes synchronizes the nodes so that they all read the commands out of memory and perform the indicated actions in unison."* and *"A reference oscillator clock signal ROSC produced by a clock circuit 25 of FIG. 1*

provides a common timing reference to all nodes 14 so that their operations may be synchronized during a test operation in a manner described below.", including the control module to minimize measurement faults and that oscillators are a well known and conventional producer of such clock signals. The Examiner further takes note that there is no invention in shifting the location of elements within a device unless there exists an unexpected result or synergistic effect from any particular claimed location. Therefore, because Ekstedt *et al.* discloses the use of generic parametric tests, because such tests are well known to include synchronous elements and because the control source of the synchronizing signal may be shifted, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Ekstedt *et al.*, as modified above, a known synchronous control signal from the control module through a conventional synchronous clock signal source to test implementation modules so as to receive the expected results expected there from, such as increased test reliability.

More particularly with respect to claim 13, 26, 41 and 56, Ekstedt *et al.* as modified above discloses the instant invention with the exception that Ekstedt *et al.* as modified above does not specify that the state oscillator module controls other modules during conventional operational superstates. Ekstedt *et al.* discloses in col. 4 that any appropriate test may be performed by the invention. The Examiner further takes note that there is no invention in shifting the location of elements within a device unless there exists an unexpected result or synergistic effect from any particular claimed location, see In re Japikse, 86 USPQ 70 (CCPA 1950). Therefore, because Ekstedt *et al.* as modified above discloses the use of synchronous control, because conventional test superstates such as abort, pause, etc. require such synchronicity and because the control source of the synchronizing signal may be shifted, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Ekstedt *et al.*, as modified above, that the state oscillator module controls other modules during conventional operational superstates so as to receive the expected results expected there from, such as increased test reliability.

As to claims 12, 25, 40 and 55, said claims are directed towards the control module controlling the state oscillator module and other modules. Ekstedt *et al.* as modified

above discloses the instant invention with the exception that Ekstedt *et al.* as modified above does not specify that the control module synchronously sets the state oscillator module and other test modules. Ekstedt *et al.* discloses in col. 4 that any appropriate test may be performed by the invention. The Examiner takes notice that parametric testing of ICs is commonly performed with clock synchronization of test modules, see Lesmeister (5,931,952) *"Thereafter a clock signal transmitted to all of the nodes synchronizes the nodes so that they all read the commands out of memory and perform the indicated actions in unison."* and *"A reference oscillator clock signal ROSC produced by a clock circuit 25 of FIG. 1 provides a common timing reference to all nodes 14 so that their operations may be synchronized during a test operation in a manner described below."*, including the control module to minimize measurement faults and that oscillators are a well known and conventional producer of such clock signals and that a control unit may control the oscillator and associated other test modules. The Examiner further takes note that there is no invention in shifting the location of elements within a device unless there exists an unexpected result or synergistic effect from any particular claimed location, see In re Japikse, 86 USPQ 70 (CCPA 1950).. Therefore, because Ekstedt *et al.* discloses the use of generic parametric tests, because such tests are well known to include synchronous elements and because the control source of the synchronizing signal may be shifted, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include within the device of Ekstedt *et al.*, as modified above, the control module synchronously controlling a state oscillator and associated test implementation modules so as to receive the expected results expected there from, such as increased test repeatability.

4. The prior art made of record but not relied upon is deemed pertinent to Applicant's disclosure.

Wang *et al.* (5,859,964) discloses overseeing semiconductor wafer manufacturing with additional sensor input.

Mullen *et al.* (6,208,904 B1) discloses controlling different wafer manufacturing equipment from a single central computer.

5. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Craig Steven Miller whose telephone number is (571) 272-2219. Central facsimile services are now available at (703) 872-9306.

The Examiner can normally be reached on Mondays through Thursdays from 6:30am-2:00pm EDT. Should repeated attempts to reach the Examiner be unsuccessful, the Examiner's Supervisor, Marc Hoff may be reached at (571) 272-2216.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Private PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig Steven Miller (ss)
04 May 2005

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